REMARKS

Applicants have carefully reviewed the Office Action dated March 14, 2006. Applicants have amended Claims 1, 2, 6, 9, 10, 13 and 14 to more clearly point out the present inventive concept. Reconsideration and favorable action is respectfully requested.

Claims 1-16 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite. The Examiner has particularly pointed out the term "a first clock rate" in the claims as being indefinite, as the Examiner does not understand the meaning thereof. The Examiner has utilized the 1980 dictionary that is distributed by Radio Shack® as support for the term that "clock rate" should be interpreted as "the rate at which a word or characters of a word (bits) are transferred from one internal computer element to another. Clock rate is expressed in cycles (in a parallel/operation machine, in words; (in a serial operation machine, in bits) per second." Applicants do not deny that the rate at which words or characters are transferred could not be done at a certain clock rate but disagrees that this is the definitive and only interpretation of a clock rate. A clock rate is merely the rate at which edges of a particular clock occur and words can be synchronized to a given clock edge such they will occur for transfer at that clock rate. In sampling clocks associated with the analog-to-digital converters, there is the concept of a "conversion cycle" wherein a main clock is utilized to generate the sampling clocks. However, each of these sampling clocks occurs at the same rate, i.e., during a conversion cycle, one clock may go high and low during that conversion cycle wherein the other clock may go low and then high, but they do so at the same clock rate and they are synchronous. This is the case with respect to the ø1 and ø2 clocks in a sampled data converter. Clock signal ø1 goes high and then low during a conversion cycle and ø2 goes from low to high and then low. As such, the rising edge (202) in Figure 2 of the present application indicates a beginning of a conversion cycle and falling edge (204) indicates the end of the of the ø1 switch being held in a closed condition. The ø2 switch is controlled at a rising edge 206 to close and the end of the open state is at the falling edge (not numbered). Thus, in the single conversion cycle, the first clock pulse will occur in the ø1 clock and the second clock pulse will occur in the ø2 clock. Each of these is referred to as a separate clock, as they each have a separate output for driving a separate node in the system.

However, the conversion cycle occurs at a certain rate and, therefore, each of these two clock signals is generated and occurs at the same rate, because all of the clock edges are synchronized to the beginning of the conversion cycle or to another edge therein. Thus, both of these pulses occur at a particular rate, *albeit* with different pulse widths and at different relative phases. As such, Applicants believe that the term "clock rate" is utilized correctly to refer to the rate at which the edges of a clock signals occur. The concept of "dumping" is merely the concept of the closing of a switch which occurs in response to the change of an edge. Thus, clearly, both ø1 and ø2 operate at the same rate. They are synchronous, since they are all synchronized to a common master clock (not shown) but they are shifted in phase from each other.

However, although Applicants believe that the term "clock rate" is used correctly, the claims have been amended to remove any concerns the Examiner might have by amending the word "clock rate" to "sampling rate." Applicants believe that this should clarify any issues in this case, but such amendment is not considered to change the meaning of the claims.

To further address the Examiner's concerns in the 112 rejection, the Examiner had a concern that "clock rate" was expressed in "cycles per second" and not the duty cycle of the clock. However, the rate is the rate at which an edge occurs to cause a switch to open or to close. Thus, the term "sampling rate" might seem to clear this up. The sampling rate with respect to the clock ø1 is the time that an action is taken in response to generation of that clock or pulse edge, i.e., it may in the transition from one state to another. The term "dumping charge from the input sampling capacitor to the non-inverting input of the amplifier at a second time and at the first clock rate" refers to the time that the switch 118 closes. It can be seen that switch 106 controlled by the first clock closes to sample and then open with subsequent closing of the switch 118 to result in dumping the charge. These occur at two different times, but they do occur at the same clock rate or sampling rate. Thus, the action of dumping and the action of sampling, although done at different times, are both done at the same rate, i.e., once during a conversion cycle which has a fixed sampling rate. Thus, Applicants believe that the claims as set forth are clear in accordance with the way that sampling clocks operate. With respect with the sampling of the feedback capacitor, the claim refers to this operation as "sampling a reference voltage onto a

feedback sampling capacitor at substantially the first clock rate" (noting that the term "clock" has been changed to "sampling"). The Examiner has misconstrued the clock rate ø1/D as being at a different rate. However, the signal "D" is a digital signal that is ANDed with the clock signal. This does not change the actual rate at which a clock signal occurs but, rather, can actually blank the clock signal in a gating process. This is described in paragraph [0010] wherein it is stated that the control signal "D" is provided for controlling which of the positive or negative reference voltages are connected to node 136 during the sampling thereof onto the feedback sampling capacitor 148. Thus, this is a gating signal and not a timing signal, i.e., it does not effect the sampling rate. As such, it would not show up in a timing diagram. This is merely a gate selection device.

With respect to the Examiner's comments regarding Claim 2, the term "shifted in phase from the first clock" refers to the fact that one clock, the ø1 clock, for example, has an edge that occurs at one time in a conversion cycle whereas the edge of the second clock occurs at a later time therein measured in degrees. For example, if the first clock were inverted, the rising edge, the edge that turns on the ø1 switch, would occur at one place in the ø1 clock cycle and the rising edge of the second clock, the inverted clock, would occur at a 180° phase shift therefrom. As long as the clocks refer to or occur in a common conversion cycle, i.e., the duty cycle is the same for each clock, then the phase shift language is applicable. Further, the Examiner has made the statement that, since these are non-overlapping clocks, they cannot be in synchronism. This is incorrect. These clocks are certainly in synchronism, as they are all referenced to the same master clock. This is the conventional operation of any sampled circuit, especially a data converter. As such, this is an incorrect statement.

With respect to Claim 9, Applicants believe that the above noted comments are applicable. The Examiner indicates that two clock signals that have different duty cycles cannot operate at the same clock rate. However, this is like saying that two pulsed clock signals having different duty cycles occurring at the same frequency do not have the same "clock rate." This would be, of course, incorrect. If a first pulse occurred at a rate of 1 MHz with a duty cycle of 10% and a second pulse occurred at a rate of 1 MHz with a duty cycle of 30%, they would both

have different duty cycles but the rate of occurrence would be identical.

The recitation "a gain control input for receiving a gain control input controller" was changed in the last amendment and, as such, it is believed that this is clear. However, the term "input" on a second occurrence has been changed to "signal." Applicants believe that this may clarify the claim.

With respect to Claim 10, this is similar to Claim 2 and the comments above are applicable.

Claims 1-16 stand rejected under 35 U.S.C. §102(b) as being anticipated by *Shin*, U.S. Patent No. 6,107,871. This rejection is respectfully traversed with respect to the claims as currently presented.

Applicants believe that *Shin* does not have the ability to change the clock rates. All of the clock signals occur at the same rate. Since the claims have been amended to replace "clock" with "sampling," Applicants believe that this clarification should distinguishes over the *Shin* reference. Again, Applicants believe that the confusion is to the Examiner's interpretation of the term "clock rate." If the Examiner requires additional information, please do not hesitate to contact the undersigned. It may be that a short conversation would clarify the terminologies in the claim.

Applicants have now made an earnest attempt in order to place this case in condition for allowance. For the reasons stated above, Applicants respectfully request full allowance of the claims as amended. Please charge any additional fees or deficiencies in fees or credit any overpayment to Deposit Account No. 20-0780/CYGL-26,655 of HOWISON & ARNOTT, L.L.P.

Respectfully submitted,
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